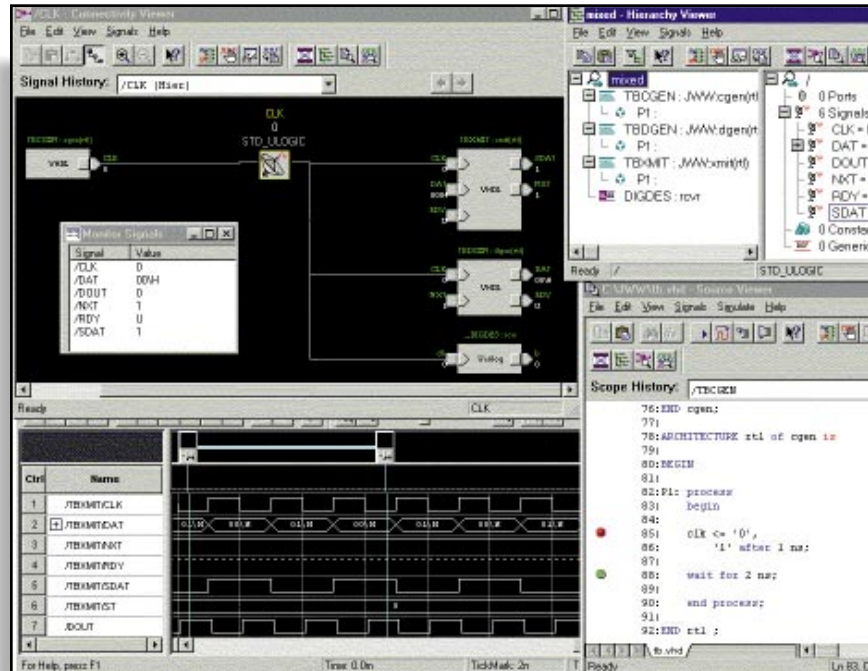


# Fusion/Speedwave™



## Highlights

- High-performance high-capacity VHDL simulation solution
- Incremental compilation reduces total compile time
- Advanced HDL debug environment increases user productivity with seamless Verilog and VHDL support
- Fully standards compliant IEEE 1076 VHDL support including VITAL for library support
- Highly accurate timing support including SDF back-annotation for post-layout timing simulation, and features to support deep sub-micron library requirements
- Widest range of ASIC and FPGA libraries available
- Extensive model support including C models, LMG HW and SW models, and Denali memory models
- Digital co-simulation with Fusion/VCS Verilog and Fusion/ViewSim gate-level simulators optional
- Mixed A/D co-simulation with ViewAnalog, Hspice or Saber simulators optional
- Tightly integrated with Viewlogic's Workview Office® Windows and Powerview® UNIX platforms
- Familiar, easy-to-use style based on standard Windows conventions with full drag-and-drop supported between all windows



## Product Overview

As designs increase in size and complexity, it is no longer enough to verify isolated parts of a design and rely on prototype debug to complete the work. Today the engineer needs a verification solution that is versatile enough to handle the entire range of verification needs from small FPGAs to large, complex systems. Viewlogic's Fusion/SpeedWave simulator is an easy-to-use, high-performance VHDL simulation system that is flexible enough to satisfy your verification and debug needs throughout the entire design process.

Fusion/SpeedWave provides the accuracy that you need to analyze complex technologies. It's versatile evaluation mechanism uses the complete IEEE 1076 VHDL language for defining arbitrary states and strengths. Fusion/SpeedWave also supports a unique 28-state algorithm to assure high-speed and high-accuracy evaluation of structural designs.

## Debugger

High-performance simulation is only half of the verification solution. If you are forced to run multiple simulations to find your design errors, total verification time can increase dramatically. The key to verification productivity is an effective debug and analysis environment. Fusion/SpeedWave provides you with the tools you need to quickly identify and track down bugs in your design.

Unlike verification solutions with limited model-import capabilities, Fusion/SpeedWave supports full visibility and control into both VHDL and Verilog design modules. Because you need to have different views of your design at different times, Fusion/SpeedWave



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supports HDL source viewing, connectivity viewing and hierarchy viewing, as well as traditional waveform viewing.

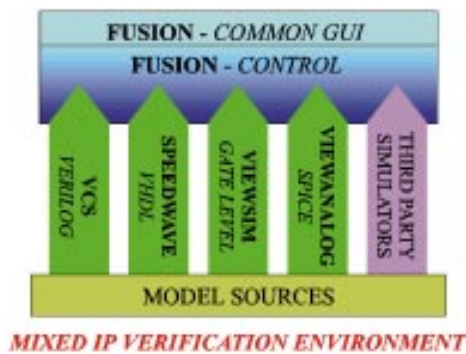
The Source Viewer displays the source HDL for any module in the design and lets you easily set breakpoints, select signals to monitor or single step through the simulation.

The Hierarchy Viewer gives you a complete view of the design hierarchy, including signals, ports, parameters, processes, etc. You can easily locate and select signals to monitor or to set breakpoints.

The most common problem with design debug is trying to find out the source of an unexpected signal value. This requires the ability to easily trace signals through the design. The Connectivity Viewer presents a graphical view of any selected signal and shows all the sources and loads, along with the current simulation values. You can easily traverse through the design from outputs to inputs and quickly discover the source of any unexpected results. This gives the user a schematic style view of the HDL design along with the current simulation results.

### Leading Vendor Libraries

Fusion/SpeedWave supports a wide range of ASIC and FPGA VHDL libraries. It provides the accurate timing simulation capabilities required for deep sub-micron libraries, and supports full SDF back-annotation for accurate post-layout design verification.



### System Simulation Solution

Viewlogic, the leading supplier of system design tools, understands the verification requirements of the system designer. A complete system verification solution must be able to support your design choices whether you are integrating IP in Verilog or VHDL, analog or digital, HDLs or schematics, or any combination. A full-range solution also needs to be able to support your choice of implementation, including ASICs, FPGAs, discrete components or any combination. The solution to system verification is Viewlogic's Fusion.

Fusion is the industry's most complete system simulation solution. Integrated into a common simulation and debug environment, designers can start with Fusion/SpeedWave and then add leading simulation engines for Verilog, schematic or analog design modules. The Fusion environment provides a common GUI for design debug, and controls the execution and communication for all of the integrated simulation engines. This gives the designers a verification solution that will support their individual design methodology without requiring any design compromises.

### Models

Fusion/SpeedWave supports the widest variety of model sources and vendor libraries. Full access to a wide range of VHDL (including VITAL) models is provided, by using co-simulation you can add support for Verilog models, ViewSim gate-level models, JEDEC, and Spice or AHDL models. This includes a wide variety of standard-part libraries as well as ASIC and FPGA vendor libraries. Standard C code support provides an interface to models and test benches created in C.

Fusion/SpeedWave supports interfaces to the Synopsys Logic Modeling Group's models. The user has access to the full range of hardware models provided by the LMG and Model Source hardware modeling systems. Popular LMG Smartmodels software models can be added to complete the simulation. Memory models from Denali can be also utilized in your VHDL design.

### Platforms

Fusion/SpeedWave is supported on a full range of popular platforms including both UNIX and Windows based systems. The tool is the same on all platforms, so the convenient features, commands and look-and-feel that you may be used to are completely available to you.



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